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IEE JNL IEE Journal or Magazine

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Zhu, Y.; Wong, W.F.;

[High Performance Computing in the Asia-Pacific Region, 2000. Proceedings. The Fourth International Conference/Exhibition on](#)

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Modeling architectural improvements in superscalar processors

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Abstract

A model of **superscalar** processors using a network of Multiple-Class-Multiple-Resource queues is described and studied. The model is able to model and study instruction classes, instruction dependencies, the cache, the **branch** unit, the **decoder** unit, the **instruction buffer**, the functional units, the retirement buffer, the retirement unit and instruction issue policy in an integrated manner. The model has been verified against measured performance and has shown an average error of 5%

Index Terms**Inspec****Controlled Indexing**[buffer storage](#) [computer architecture](#) [instruction sets](#) [performance evaluation](#) [queueing theory](#)**Non-controlled Indexing**[Multiple-Class-Multiple-Resource queues](#) [architectural improvement modeling](#) [average error](#) [branch unit](#) [central instruction buffer](#) [decoder unit](#) [functional units](#) [instruction classes](#) [instruction dependencies](#) [issue policy](#) [measured performance](#) [retirement buffer](#) [retirement unit](#) [superscalar processors](#)**Author Keywords**

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